REMARKS

Claims 3, 8-16, 24-26 and 30 are all the claims remaining in this application.

Applicant thanks the Examiner for approving the proposed drawing corrections submitted on August 29, 2002. Submitted herewith are 3 sheets of drawings which incorporate those changes approved.

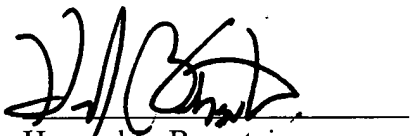
Applicant thanks the Examiner for allowing claims 8-16. Applicant also thanks the Examiner for indicating that claims 3, 24-26 and 30 contain allowable subject matter and would be allowed if written in independent form. Accordingly, claims 3, 24-26 and 30 have been amended to independent form and are now in condition for allowance.

As all the claims remaining in this application have been allowed or are now in condition for allowance, this application should be passed to issue at the earliest possible time.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: February 21, 2003

APPENDIX
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please cancel claims 1, 2, 4-7, 22, 23 and 27-29 without prejudice or disclaimer.

The claims are amended as follows:

3. (Amended) [The semiconductor device as set forth in claim 1]A semiconductor device having a plurality of wiring layers in a multi-layered structure,

the semiconductor device including an inner area (11) at a surface and a pad area (13) surrounding the inner area (11) therein,

characterized in that the semiconductor device includes a device fabricated below the pad area (13), further comprising a second device fabricated below the device,

the device being comprised of a bypass capacitor (19),

the second device being comprised of at least one of a protection device (31) and an input/output device (12).

24. (Amended) [The semiconductor device as set forth in claim 1]A semiconductor device having a plurality of wiring layers in a multi-layered structure,

the semiconductor device including an inner area (11) at a surface and a pad area (13) surrounding the inner area (11) therein,

characterized in that the semiconductor device includes a device fabricated below the pad area (13), wherein said device comprises an input/output device.

25. (Amended) [The semiconductor device as set forth in claim 1]A semiconductor device having a plurality of wiring layers in a multi-layered structure,

the semiconductor device including an inner area (11) at a surface and a pad area (13) surrounding the inner area (11) therein,

characterized in that the semiconductor device includes a device fabricated below the pad area (13), further comprising a second device fabricated below said device,

said device comprises a bypass capacitor,

said second device comprises a protection device.

26. (Amended) [The semiconductor device as set forth in claim 1]A semiconductor device having a plurality of wiring layers in a multi-layered structure,

the semiconductor device including an inner area (11) at a surface and a pad area (13) surrounding the inner area (11) therein,

characterized in that the semiconductor device includes a device fabricated below the pad area (13), further comprising a second device fabricated below said device,

said device comprises a bypass capacitor,

said second device comprises an input/output device.

30. (Amended) [The semiconductor device as set forth in claim 28]A semiconductor device having a plurality of wiring layers in a multi-layered structure,

the semiconductor device including an inner area (11) at a surface and a pad area (13) surrounding the inner area (11) therein,

characterized in that the semiconductor device includes a device fabricated below the pad area (13),

wherein said device comprises a bypass capacitor,

wherein said bypass capacitor comprises metal wire layers arranged below said pad area,

wherein each of said metal wire layers comprises a first wire and a second wire with an interlayer insulating layer being sandwiched therebetween,

said first wire being electrically connected to a voltage source,

said second wire being grounded, further comprising at least one of first to fourth pads in said pad area,

said first pad being electrically connected to an input/output device,

said second pad being electrically connected to said first wire,

said third pad being electrically connected to said second wire,

said fourth pad being not electrically connected to said input/output device, said first wire and said second wire.